Identification

Major Module Port Assignment
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Purpose

This section describes a standard way to connect cables between
major modules at 645 Multics installations. Also, standard
nomenclature and conventions are introduced for discussing
port assignments. The standard connections listed here
are based on three considerations:

1. Hardware restrictions

2. Software restrictions

3. Consistency, to simplify reconfiguration

The connections described in this section apply to the
maximum configuration in use at a given installation and
include all physical equipment available at that installation.
These cable connections are not changed when the system
is electrically reconfigured for system testing or hardware
malfunction.

System Controllers

Each System Controller has a maximum of eight ports to
which active modules may be connected. These ports are
numbered 0, 1, 2, etc., in decreasing order of priority.
Starting with port 0, active modules are attached to System
Controller ports in the following order:

$$
\left.\begin{array}{l} \text{EMM } \#1 \\ \text{EMM } \#2 \\ \text{ etc.} \end{array}\right\} \quad \text{all EMM's}
$$
$$
\left.\begin{array}{l} \text{GIOC } \#1 \\ \text{GIOC } \#2 \\ \text{ etc.} \end{array}\right\} \quad \text{all GIOC's}
$$
$$
\left.\begin{array}{l} \text{CPU } \#1 \\ \text{CPU } \#2 \\ \text{ etc.} \end{array}\right\} \quad \text{all CPU's}
$$

This pattern is repeated identically for every System Controller.

Active Modules

Each active module has a maximum of eight ports, lettered A, B,
C, etc., to which System Controllers may be connected.
All active modules are connected to system controllers
identically, as follows: port A of each active module
is connected to System Controller 1; port B to System

Controller 2, etc., up to the maximum number of System
Controllers at the installation.

Special Processor Port Assignment

(This paragraph to be deleted when Prototype System Clock
is no longer used with 645 systems.)

Whenever a system contains one or more prototype system
clocks, each system clock appears to reside in its own
System Controller; no core memory exists in this special
clock controller. A system using prototype system clocks
may not have more than two processors, since the special
clock controllers have only two ports. We assume here
that a system does not contain more than two prototype
clocks. The eight processor ports are assigned as in
table 1 when prototype clocks are used. If prototype
clocks are not used, processor ports are assigned exactly
the same as all other active modules.

Example

Figure one illustrates the cable assignment for a system
containing four system controllers, one EMM, two processors,
and two prototype system clocks.

Processor Port	Connects to		
	2-controller system	4-controller system	6-controller system
A	Clock 1	Clock 1	Clock 1
B	Clock 2	Clock 2	Clock 2
C	(unused)	(unused)	controller 5
D	(unused)	(unused)	controller 6
E	controller 1	controller 1	controller 1
F	controller 2	controller 2	controller 2
G	(unused)	controller 3	controller 3
H	(unused)	controller 4	controller 4

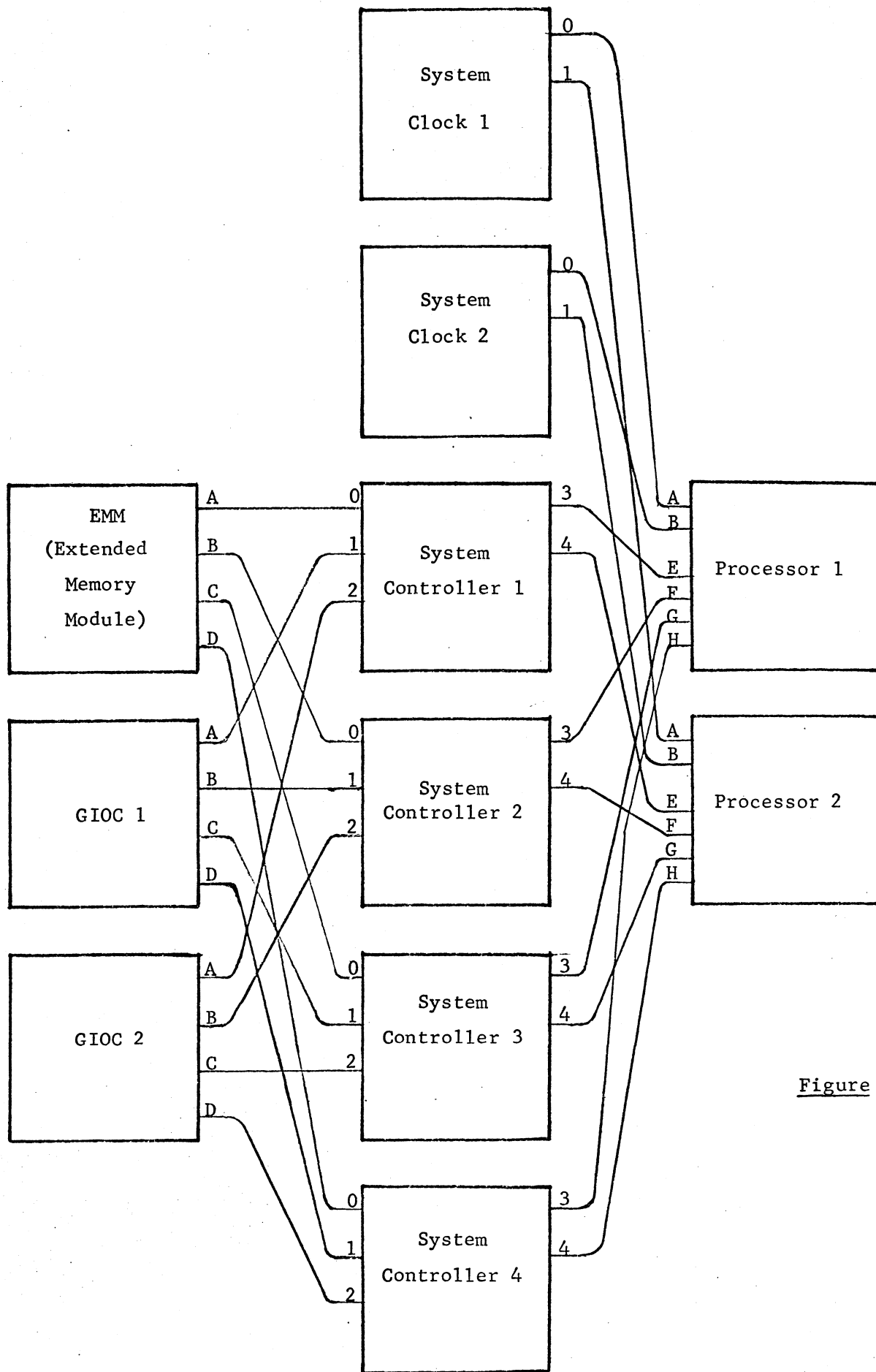Table I: Processor Port connection when prototype clocks are used.

Figure 1.