TO: Operations

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SUBJECT: Memory **read** procedure for parity errors

This writeup is to assist operations in determining the "Memory Configuration"

portion of the Multics Error Report Form.

A.   Put processor in step

B.   At Memory:

   1.   Test Switch in test (down)

   2.   Command switches <u>all down</u>

   3.   Stop on faultswitch down

   4.   Increment address switch down

   5.   Increment counter switch down

   6.   Display select switch in "ADDR REG" position

   7.   "RPT" "START" switch in center position.

This procedure will start memory in a read loop. If memory should stop find fault as

indicated and note address.

C.   Reset all switches

D.   Processor back into run

Under normal conditions the internal portion of all memories will be kept low. The

Core Assignment switches should be set as follows: ↑↑↓↓↑↑↓↓

If it is necessary for the external portion to be low the switches should be: ↓↓↑↑↓↓↑↑

On mem G the Core Assignment Switches are set vertically rather than horizontally

as on F and H.